An Image Sensor Which Captures 100 Consecutive Frames at 1 000 000 Frames/s

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***Abstract*—An image sensor for a video camera of 1 000 000 frames per second (fps) was developed. The specifications of the developed sensor are as follows: 1) frame rate: 1 000 000 fps; 2) pixel count: 81 120 ($= 312 \times 260$) pixels; 3) total number of successive frames: 103 frames; 4) gray levels: 10 b; and 5) open area of each pixel (fill factor): 580 square micrometers (13%). The overwriting function is installed for synchronization of image capturing with occurrence of the target event. Sensitivity is significantly high with the large photogate. Some innovative technologies were introduced to achieve ultrahigh performance, including slanted linear CCD *in situ* storage, curving design procedure, and a CCD switch with fewer metal shunting wires. They are applicable to the development of other new high-performance image sensors.**

***Index Terms*—CCD, high-speed, image sensor, in situ storage.**

I. Introduction

In 1991, the authors [1] developed a video camera of 4500 frames per second (fps). The maximum frame rate with a reduced pixel count was 40 500 fps. It was the first high-speed video camera with full digital memory, no mechanical parts, and 16 parallel readout taps. The camera became the defacto standard high-speed video camera and has been used worldwide in scientific and engineering applications such as the KODAK HS4540 and Photron FASTCAM.

Soon after the development of the camera, there were claims that the frame rate was insufficient. In 1993, the authors distributed 1000 questionnaires to potential users of high-speed video cameras in Japan to find out users' requirements in high-speed image capturing [2]. In 2000, similar questionnaires were distributed to 3000 potential users. One of the results from the questionnaires, the expected frame rate, is shown in Fig. 1. It shows that, in 1993, the frame rate of 4500 fps satisfied 40% of potential applications, and 1 000 000 fps covered 95%. During the seven years from 1993 to 2000, the expected frame rate has gradually increased. Currently, the frame rate of 1 000 000 fps satisfies 85% of potential applications. The questionnaires provided useful information about users' requirements for other performance indices of high-speed image sensors, such as expected consecutive frame numbers, pixel count, and dynamic range. The specifications of the present sensor were defined on the basis of the results.

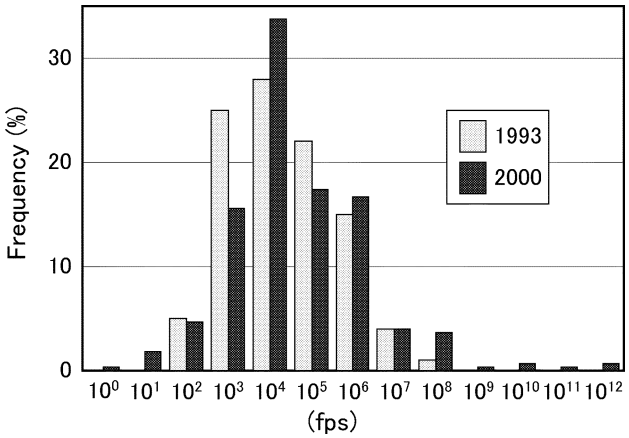

Fig. 1. Temporal tendency on expected frame rate from 1993 to 2000.

Because it is virtually impossible to achieve 1 000 000 fps by means of parallel readout, a new concept, the "In situ Storage Image Sensor (ISIS)," was introduced for the development of a video camera capable of more than 1 000 000 fps [3], [4]. A local memory is built within or beside each pixel of the ISIS. The memory size should be sufficiently large to reproduce a moving image. During an image capturing operation, image signals generated in the photodiode of each pixel are recorded in the *in situ* storage. The recording operation is done in all pixels in parallel. The ultimate parallel operation achieves the theoretically highest frame rate.

The development project of the ISIS by the authors began in 1999, upon notification by the Japanese government of its financial support. The sensor and the camera mounting the sensor were developed in 2001. Innovative technologies were also developed and introduced to maximize the performance of the sensor, including slanted linear CCD *in situ* storage, curving design procedure, and a CCD switch with fewer metal shunting wires. This paper describes the structure, operation, supporting technologies, and performance of the ISIS.

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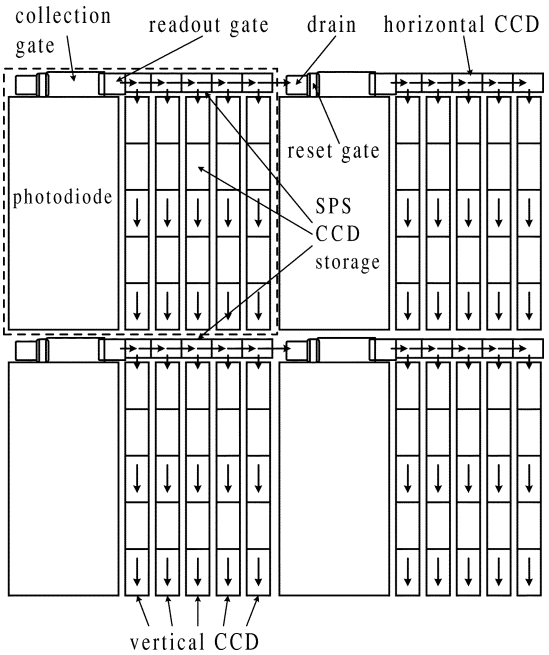

Fig. 2. Burst image sensor; ISIS with the SPS CCD storage [5].

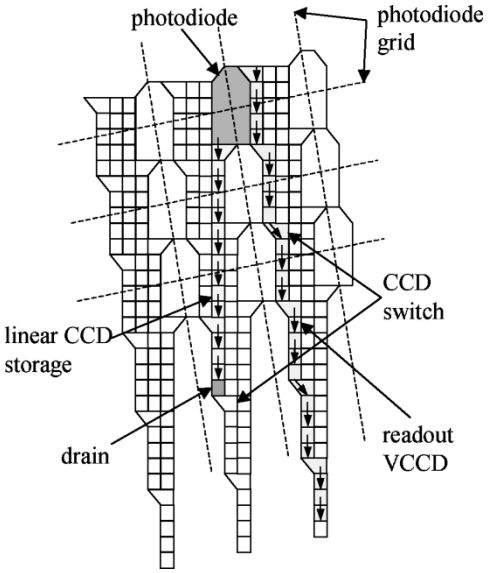

Fig. 3. Elements of an ISIS with slanted linear CCD storage.

II. Serial-Parallel-Serial Versus Slanted Linear CCD Structures for *In Situ* Storage

A. In Situ Storage Image Sensor

The *in situ* storage for ultrahigh-speed image capturing is not entirely a new idea. Some proposals have been presented for the structure. Simplification of the structure of the *in situ* storage has been the key technology. The *in situ* storage is installed in a very small area within or beside a pixel. The simplest structure minimizes the area of one storage element and maximizes the number of the storage elements installed in a pixel, which is equal to the number of consecutive frames. For a fixed number of storage elements, the smaller storage elements reduce the area of a pixel and increase the number of pixels installed in the limited photo-receptive area of an ISIS. Therefore, a simpler structure increases the number of consecutive frames or the spatial resolution of the sensor. Yield rate and noise level are decreased by the simpler structure.

B. Serial-Parallel-Serial CCD Storage

Kosonosky *et al.* developed "a burst image sensor" [5]. They introduced "Serial-parallel-serial CCD (SPS-CCD)" to the design of the *in situ* storage. The design was simple and elegant, as shown in Fig. 2. A drain was installed beside each *in situ* storage for overwriting. The overwriting function is essential for the *in situ* storage image sensors. Since the number of the storage elements is relatively small and the image capturing operation is very fast, the overwriting drastically eases the synchronization of image capturing with occurrence of the target event.

The elegant design, with the SPS-CCD *in situ* storage, seemed the ultimate ISIS design. However, it had one disadvantage, as pointed out later by the authors, namely the two-directional charge transfer. Charge packets are transferred horizontally on a horizontal CCD register, vertically on parallel vertical CCD registers, and horizontally again within a small *in situ* storage area. As a result, the number of storage elements was 30, which was not sufficient to reproduce moving images; the pixel count also remained at 190×190 pixels due to the extremely low yield rate. Swain *et al.* developed the SPS-CCD ISIS with higher frame rate [6], following Kosonocky's original work [5].

C. Slanted Linear CCD Storage

Most previous proposals on the ISIS, including the SPS-CCD ISIS, employed the *in situ* storage within a pixel. The simplest CCD structure is linear, without bends. If the linear CCD is employed as the *in situ* storage and the number of storage elements is sufficiently large, the linear CCD storage extends outside of the pixel, violating the area of neighboring pixels. The basic approach in the development of the proposed ISIS was as follows: assume the linear CCD *in situ* storage and devise a suitable layout to incorporate the linear CCD structure with other basic functions of the ISIS, such as overwriting function and square pixel grid. This was achieved by the introduction of the "slanted linear CCD storage."

III. ISIS With Slanted Linear CCD Storage

A. Structure

A new ISIS structure is proposed. The structure is schematically explained in Fig. 3. The number of CCD storage elements in the figure is 15 (there are, in fact, 103 such elements). The sensor employs the four-phase transfer to maintain sufficient charge-handling capacity. The transfer scheme requires a set of four metal wires. The quasi-two-phase transfer can be applied by using four electrodes on each CCD element, which increases the frame rate by four times, while sacrificing the charge-handling capacity.

1) Pixel Components: The element structure is basically composed of a large photodiode, a CCD storage extending linearly downward from the photodiode, a drain for overwriting at the lower end of the storage, and a CCD switch for the

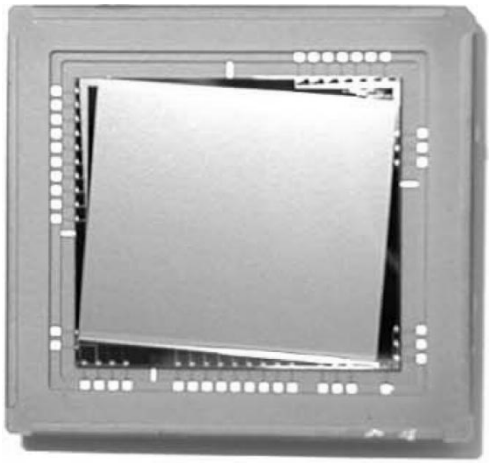

Fig. 4. Prototype of the ISIS (tfhe packaging is slanted).

readout operation. The storage area is covered with a metal light shield.

2) Photogates: High sensitivity is achieved by very large photodiodes, compared to the size of a CCD element in the linear storage. Membrane electrodes are placed on each photodiode. The photodiode, covered with the electrodes, works as a photogate. Different voltages are applied to the electrodes on the photogate, which creates a potential gradient in the photodiode toward the input gate to the linear CCD storage. The potential gradient increases transfer velocity of electrons in the photogate and, thus, the frame rate. By changing the voltages applied to the electrodes, electrons accumulated in the photodiode can be drained to the substrate, which makes possible the complicated electronic shuttering operation required in scientific and engineering applications. The membrane electrodes covering the photodiode reduce the amount of blue light reaching the photodiode. The disadvantage is compensated for by the increased frame rate and the introduction of the complicated electronic shuttering operation. The center of a pixel is the center of the photogate. The pixels are placed on a square grid.

3) Slanted Linear CCD Storage: The linear CCD *in situ* storage also consists of a square array, which simplifies the design of the CCD storage. The slightly slanted alignment of the CCD array to the pixel array makes possible that both the pixel and the CCD storage arrays are square. The one-directional transfer CCD storage significantly simplifies the structure of the gates and metal wiring within the *in situ* storage, compared to the SPS structure. Thus, the area of the *in situ* storage is minimized and the number of stored consecutive images is maximized. The simplicity of the structure also contributes to the increased yield and the decreased noise. A photo of the developed sensor is shown in Fig. 4, in which the chip is mounted on a package in a slightly slanted position. The pixel grid then becomes square when the package is mounted on a camera.

4) Overwriting Drain: An overwriting gate is installed at the end of each linear CCD storage. The structure is a standard vertical drain to the substrate.

5) Readout VCCD and CCD Switch: For readout, a CCD channel beside each photogate is used as a readout vertical CCD segment. The segments are connected by small steps. Each step

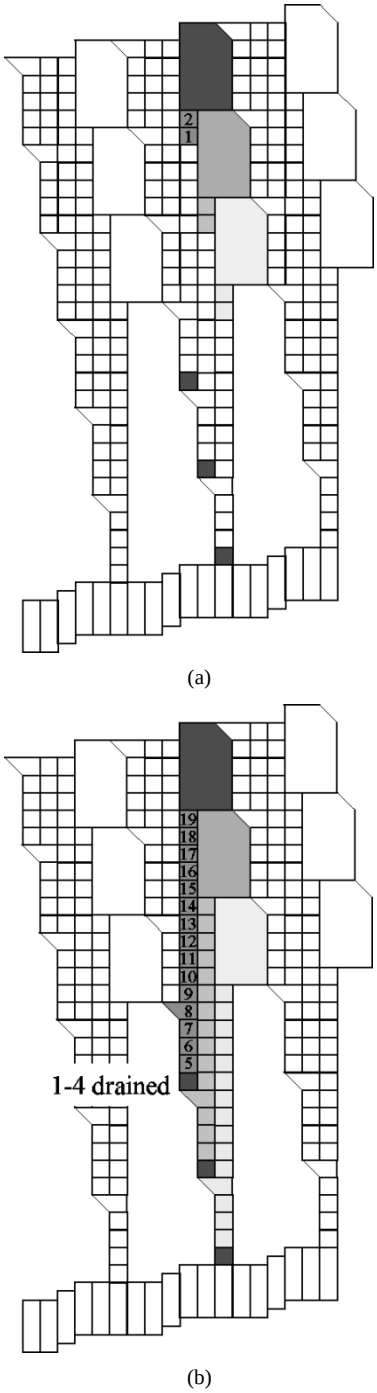

Fig. 5. Image-capturing operation. (a) Recording operation at the first stage. (b) Recording/overwriting operation.

works as a CCD switch to select the transfer of image signals to a readout VCCD segment, either from the upper readout VCCD segment or from the upper in situ storage segment. The overwriting drain gate functions as a normal transfer CCD element during a readout operation, following the image capturing operation.

To independently operate the storage CCD and the readout VCCD, four metal wires should be placed on the one VCCD channel, forming closely spaced adjacent metal wires. The small distance between metal elements significantly reduces the yield rate. A new structure and associated operation scheme

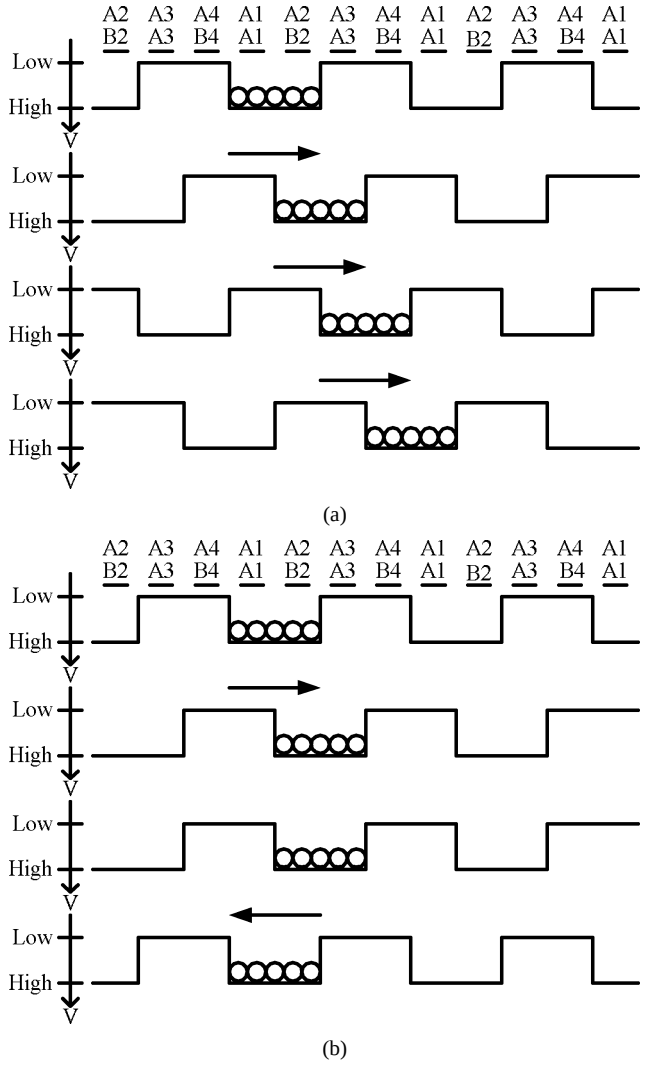

Fig. 6. Operations of two adjacent independently operated CCD channels of four-phase transfer (six electrodes are placed; two electrodes, A1 and A3, are used in common). (a) Transfer phase. (b) Reservation phase.

are proposed to solve the problem. The proposed scheme requires only two additional metal wires on the readout VCCD of the four-phase transfer. The operation scheme is explained in Section III-B2.

B. Operation

1) Image Capturing Operation: During an image-capturing operation, image signals generated in the photodiode of a pixel are recorded in the *in situ* storage, as shown in Fig. 5(a) and (b). The recording operation continues in parallel in all pixels, achieving the ultimate high-speed image capturing.

As shown in Fig. 5(b), overwriting operation continues during the image-capturing operation, draining old image signals to the outside of the sensor and keeping a sequence of the latest image signals in the *in situ* storage, which substantially eases the synchronization of image capturing with occurrence of the target event in the ultrahigh-speed image capturing.

2) Readout Operation: When a target event is detected, the image-capturing operation with overwriting is stopped, and the past image sequence recorded in the *in situ* storage is read out of the sensor and reproduced as a moving image. The readout operation is as follows.

1) Only image signals stored in the readout VCCD are transferred to the HCCD, placed below the photo-receptive area, keeping image signals in the *in situ* storage without transfer. The readout VCCD becomes empty.

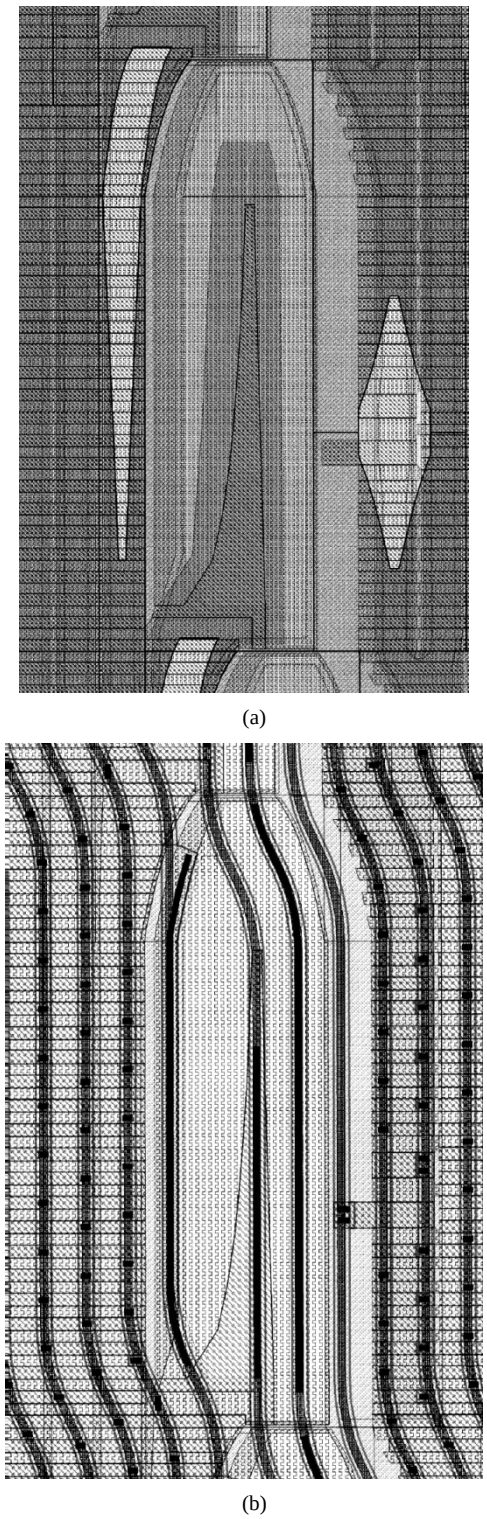

Fig. 7. Part of the design: beautiful curves are applied: (a) doping and electrodes and (b) electrodes and metal wires.

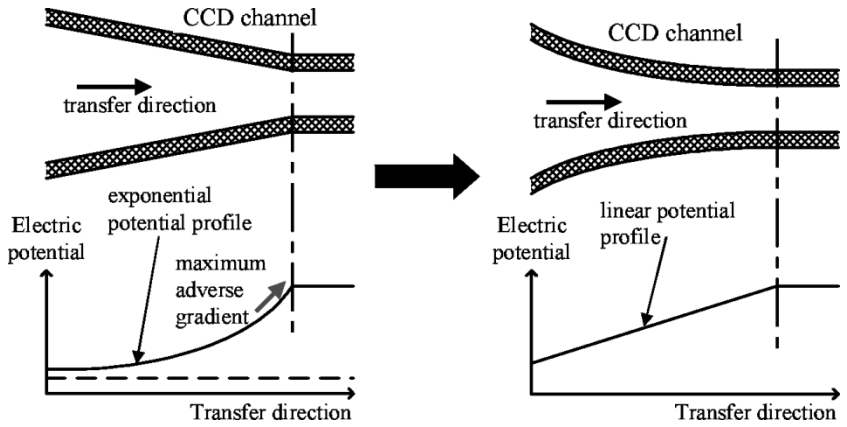

Fig. 8. Optimum shape of a narrowing channel: (a) narrowing CCD channel and (b) logarithmic CCD channel (inverse of the exponential curve).

2) Image signals in the storage are transferred to the empty readout VCCD until it is full. The cyclic operation of 1) and 2) continues until the storage and the readout VCCD are empty.

Though four-phase transfer is applied to both the *in situ* storage and the readout vertical CCDs, the number of metal wires on the readout VCCD is two, as explained before in Section III-A5. The readout operation is achieved by the scheme shown in Fig. 6.

The linear CCD storage is operated with a set of four electrodes, A1, A2, A3, and A4, while the readout VCCD is operated with A1, B2, A3, and B4. Two of four electrodes, A1 and A3, work in common, and two additional electrodes, B2 and B4, are placed on the readout VCCD, instead of A2 and A4.

Transfer voltage patterns for A1 and A3 are the same as the standard four-phase transfer. When voltage patterns for A2 and A4 (or B2 and B4) are the same as the standard transfer, charge packets are simply transferred [Fig. 6(a)].

If the voltage of A2 (or B2) is fixed at the higher level and that of A4 (or B4) at the lower level, A4 (B4) works as a blocking gate and A2 (B2) as a reserving gate, and a charge packet is kept beneath [A1 and A2] or [A2 and A3] (or [A1 and B2] or [B2 and A3]) alternately [Fig. 6(b)]. Consequently, without B1 and B3, the linear CCD storage and the readout VCCD are independently operated either as transfer CCD or as storage CCD.

C. Curving Design

A part of the design of the developed ISIS is shown in Fig. 7. Curving design is introduced to the elements, instead of the standard rectangular design. The curving design improves potential profiles. The advantage of the curving design is explained below, using "narrowing channel" and "large photogate with curving electrodes" as examples.

1) Narrowing Channel: The example shown in Fig. 8 is a narrowing CCD channel. If the channel width is linearly reduced, the adverse potential gradient increases gradually, becoming steepest at the end of the narrowing part. The steepest adverse gradient makes transfer of electrons most difficult. The best shape of the potential profile along the transfer direction is achieved by minimizing the maximum adverse gradient, i.e., by a straight line. If we move to the left in Fig. 8(a), the channel width linearly increases. The potential then approaches an asymptotic constant value. The potential profile can be approximated by an exponential curve. The shape of the channel which makes the potential profile linear was theoretically derived as the inverse expression of the exponential curve, i.e., a logarithmic curve.

TABLE I
DESIGN SPECIFICATION OF THE TEST ISIS

Frame Rate	1,000,000 fps (max)
Pixel Count	312x260 (= 81,120) pixels
Pixel Size	66.3x66.3 microns^2
Size of CCD Element	5.1x5.1 microns^2
Fill Factor (Area of Photogate)	13 % (580 microns^2)
Number of Stored Image	103 frames
Charge Handling Capacity	25,000 electrons
Grey Level	10 bits
Overwriting Drain	Installed
Transfer Scheme	4-phase transfer (Quasi 2-phase transfer for HCCD)
Temperature of the Sensor	0 − 5℃ (Cooled by Peltier Device)

2) Large Photogate: The photodiode is extremely large and thus provides very high sensitivity. The shape of an electrode on the photodiode for increasing the electron transfer speed is also logarithmic, in this case, increasing the width along the transfer direction. If it linearly increases, the potential profile at the lowest end becomes very flat, which makes the potential gradient nearly zero and decreases the transfer velocity of generated electrons. The logarithmic shape provides a favorable linear potential profile, which maximizes the minimum potential gradient and maximizes the transfer velocity of electrons.

Kosonocky *et al.* [5] employed an additional three-step n-doping to increase the transfer speed on the large photodiode. The concentration of the n-type doping becomes denser toward the outlet of the photodiode. This results in the following two problems: additional doping processes are necessary to a standard CCD process, and, since the potential at the outlet becomes too deep, an additional input gate is necessary for the operation to carry the electrons up from the deep well to the

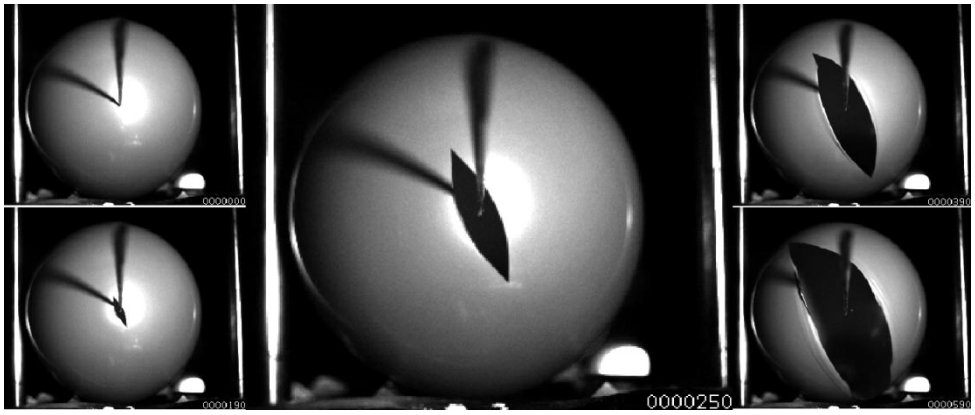

Fig. 9. Bursting balloon (frame rate: 100 000 fps) (the large image at the center is for evaluation of the image quality).

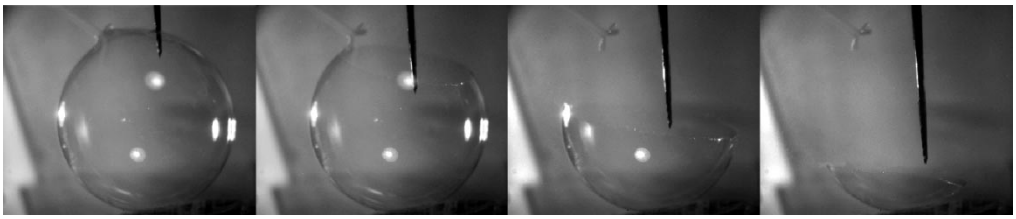

Fig. 10. Bursting soap bubble (frame rate: 5000 fps).

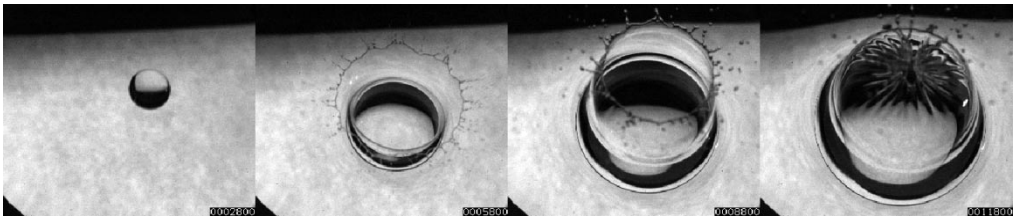

Fig. 11. Water crown generating a surface bubble (frame rate: 5000 fps).

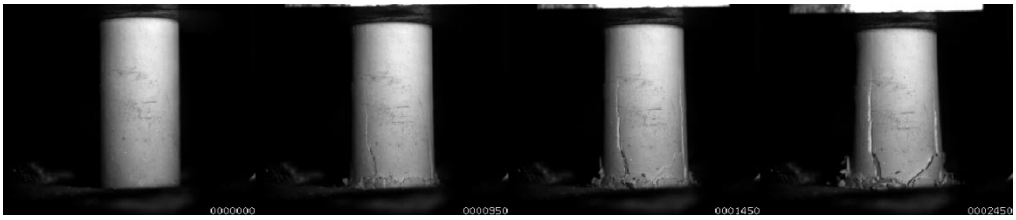

Fig. 12. Fracturing of a plaster column (frame rate: 20 000 fps).

CCD channel. The logarithmic electrode on the photodiode eliminated the problems.

The curving or nonrectangular design was also employed in the "Honeycomb CCD [7]." The curving design will become a standard design procedure for developing higher performance image sensors and ICs. The design of the proposed ISIS was largely supported by a three-dimensional (3-D) device simulator "SPECTRA." An IC-CAD applicable to curving design is expected to be developed.

D. Performance of the Developed ISIS

Design specification of the test sensor is shown in Table I.

The maximum frame rate is 1 000 000 fps and the pixel count is 81 120 $(= 312 \times 260)$ pixels. The total number of the successive frames is 103 frames. The fill factor is only 13%. The area of the photogate is, however, sufficiently large to provide high sensitivity. Attachment of a cylindrical on-chip microlens array on the sensor drastically increases the sensitivity. The overwriting function is installed.

E. Cameras and Example Images

The camera mounting the test sensor was developed and applied to capture example images. The examples, shown in Figs. 9–12, are of a bursting balloon (taken at 100 kfps), a bursting soap bubble (taken at 5 kfps), a water crown generating a surface bubble (taken at 5 kfps), and the fracturing of a plaster column (taken at 20 kfps). They are reproduced as moving images at 10 fps for 10 s, which is sufficient to activate the dynamic recognition of scientists and engineers.

A triple-ISIS camera has been developed that provides either a color version with 243 360 $(= 3 \times 81{,}120)$ pixels or a monochrome version with consecutive 309 $(= 3 \times 103)$ frames for the reproduction of moving images at 30 fps for 10 s or at 10 fps for 30 s.

IV. Concluding Remarks

An image sensor for a video camera of 1 000 000 fps was developed. The specifications of the developed sensor are as follows: 1) frame rate: 1 000 000 fps; 2) pixel count: 81 120 $(= 312 \times 260)$ pixels; 3) total number of successive frames: 103 frames; 4) gray levels: 10 b, and 5) fill factor and the effective open area of the photogate: 13% and 580 square micrometers. The overwriting function is installed for the synchronization of image capturing with occurrence of the target event. Sensitivity is significantly higher with the large photogate.

Some innovative technologies were introduced to achieve the ultra-high performance, including slanted linear CCD *in situ* storage, curving design procedure, and a CCD switch with fewer metal shunting wires.

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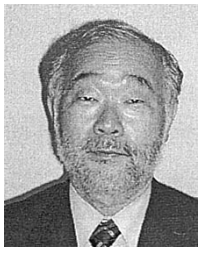

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Albert J. P. Theuwissen (SM'95–F'02) was born in Maaseik, Belgium, on December 20, 1954. He received the degree in electrical engineering from the Catholic University of Leuven, Belgium, in 1977. His thesis work was based on the development of supporting hardware around a linear CCD image sensor. He received the Ph.D. degree in electrical engineering in 1983. His dissertation was on the implementation of transparent conductive layers as gate material in the CCD technology.

From 1977 to 1983, his work at the ESATLaboratory of the Catholic University of Leuven focused on semiconductor technology for linear CCD image sensors. In 1983, he joined the MicroCircuits Division of the Philips Research Laboratories, Eindhoven, The Netherlands, as Member of the Scientific Staff. Since that time he was involved in research in the field of solidstate image sensing, which resulted in the project leadership of respectively SDTV- and HDTVimagers. In 1991, he became Department Head of the Imaging Devices division, including CCD as well as CMOS solidstate imaging activities. He is author or coauthor of many technical papers in the solidstate imaging field and issued several patents. He is member of editorial board of the magazine *Photonics Spectra*. In March 2001, he became part-time Professor at the Delft University of Technology, the Netherlands, where he teaches courses in solid-state imaging and coaches Ph.D. students in their research on CMOS image sensors. In 1995, he authored a textbook *Solid State Imaging with Charge Coupled Devices*.

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