An image sensor of 1,000,000 fps, 300,000 pixels, and 144 consecutive frames

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ABSTRACT

An image sensor for an ultra-high-speed video camera was developed. The maximum frame rate, the pixel count and the number of consecutive frames are 1,000,000 fps, 720 x 410 (= 295,200) pixels, and 144 frames. A micro lens array will be attached on the chip, which increases the fill factor to about 50%. In addition to the ultra-high-speed image capturing operation to store image signals in the in-situ storage area adjacent to each pixel, standard parallel readout operation at 1,000 fps for full frame readout is also introduced with sixteen readout taps, for which the image signals are transferred to and stored in a storage device with a large capacity equipped outside the sensor. The aspect ratio of the frame is about 16 : 9, which is equal to that of the HDTV format. Therefore, a video camera with four sensors of the ISIS-V4, which are arranged to form the Bayer's color filter array, realizes an ultra-high-speed video camera of a semi-HDTV format.

Keywords: high-speed video camera, ISIS, in-situ storage image sensor, ultra-high-speed, high spatial resolution

1. INTRODUCTION

In 2001, the authors developed an image sensor of 1,000,000 fps and a video camera mounting it[1),2)]. The sensor was named "ISIS-V2", the in-situ storage image sensor, version 2. They were a test sensor and a test camera with a relatively small number of pixels, i.e., 81,120 pixels (260x312) and a relatively small number of consecutive frames, i.e., 103 frames. All the pixel of the seonsor has an in-situ memory area with 103 CCD memory elements, and a drain. In an image capturing operation, image signals are simultaneously stored in the in-situ storage at all the pixels. The ultimate parallel recording achieved the ultimate high-speed image capturing. When the in-situ storage becomes full of image signals, the oldest one is drained through the drain to the substrate and the newest one is stored instead. With this overwriting operation, the latest consecutive image signals are always stored in the in-situ storage, continuously draining the old ones. The overwriting operation continues until a target event occurs and a trigger signal to stop the image capturing operation is released to the sensor. Then, the image signals stored in the in-situ storage are slowly readout from the sensor to a buffer memory outside the sensor. The overwriting operation significantly eases synchronization of image capturing with occurrence of the target event, especially for the camera system with a storage area for relatively small number of frames, such as the ISIS camera.

In 2001, an image sensor of 1,000,000 fps for practical use was developed, called ISIS-V4. The pixel count is about

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300,000 (= 410x720) pixels and the number of consecutive frames is 144. In addition to the simultaneous in-situ storage operation mode, the sensor equips with function for parallel readout operation mode with sixteen readout taps, which enables continuous readout of image signals from the sensor to a storage device at 1,000 fps for the full frame readout. An on-chip micro lens array will be also mounted on the sensor chip, which will significantly increase the fill factor to about 50%. The aspect ratio of the frame is about 16 : 9, which is equal to that of the HDTV format. Therefore, a video camera with four sensors of the ISIS-V4, which are arranged to form the Bayer's color filter array, realizes an ultra-high-speed video camera of a semi-HDTV format.

This paper outlines the development history of the design of the ISIS-V4. At first, the basic structure and the basic operations of the ISIS-V2, developed in 2001, are briefly explained, which may be helpful to understand the functions of the ISIS-group. Then, the ISIS-V3 is explained, which was designed with major changes from the ISIS-V2 and is the basic model of the ISIS-V4. Finally, the special features of the ISIS-V4 are briefly explained, which was designed for NHK, the Japan Broadcasting Corporation, with some changes from the ISIS-V3 to meet requirements to be satisfied as an ultra-high-speed video camera for broadcasting.

2. A PREVIOUSLY-DEVELOPED ULTRA-HIGH-SPEED IMAGE SENSOR: ISIS-V2

2.1. Basic structure

Before explaining the ISIS-V4, it may be better to briefly explain the ISIS-V2, the original image sensor for an ultra-high-speed video camera of 1,000,000 fps. While the appearances of the design looks different from that of the ISIS-V4, the structure and the operations are basically the same. It is easier to understand the principles from the original configuration before addition of many improvements.

The basic structure and the packaged sensor of the ISIS-V2 are shown in Fig.1 and Fig. 2. One pixel element is composed of a large photodiode, an in-situ CCD storage channel stretching downward from the photodiode, and a drain attached at the end of each CCD storage channel. The center of a pixel is at the center of each photodiode, consisting of a pixel grid, which is slightly slanted to the CCD grid. The photoreceptive area is composed of the pixel array and vertical readout CCD channels with short bends stretching beside each column of the photodiodes. A vertical readout CCD consists of a string of the last segments of in-situ CCD storage elements connected with CCD switches. The sensor consists of the photoreceptive area, one horizontal readout CCD channel, a diffusion amplifier and a readout tap which are not shown in the figure.

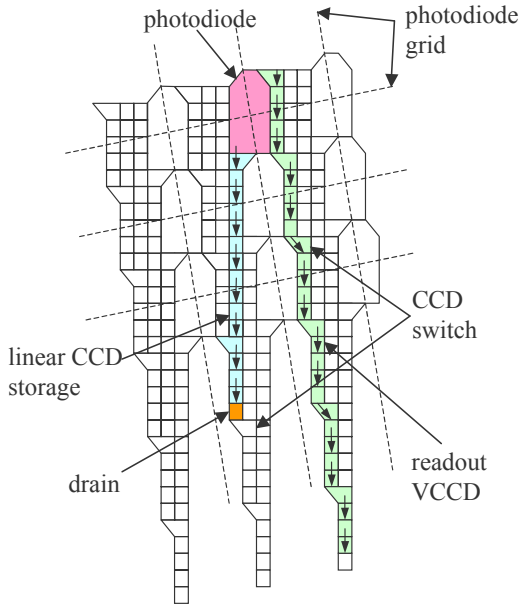


Fig. 1 The basic structure of an ISIS

Fig. 2 A photograph of a packaged ISIS
The chip is packaged with rotation of a small angle to compensate the slanted configuration of the photodiode/pixel grid shown in Fig 1.

The size of the photodiode is very large, compared to that of the CCD element, which provides the sensor with very high sensitivity for ultra-high-speed imaging. Though the pixel grid is slanted, it becomes square with horizontal and vertical axes by packaging the chip with slight rotation, as shown in Fig. 2.

Each storage area consists of fifteen CCD elements, which makes it possible to simultaneously store image signals for consecutive fifteen frames. The complete parallel recording provides the ultimate ultra-high-speed continuous image capturing. The number of CCD elements of the actual ISIS-V2 is one hundred three, instead of fifteen.

The pixel count is 312x260 (= 81,120). The sizes of the CCD elements and the pixel are 5.1x5.1 micron^2 and 66.3x66.3 micron^2.

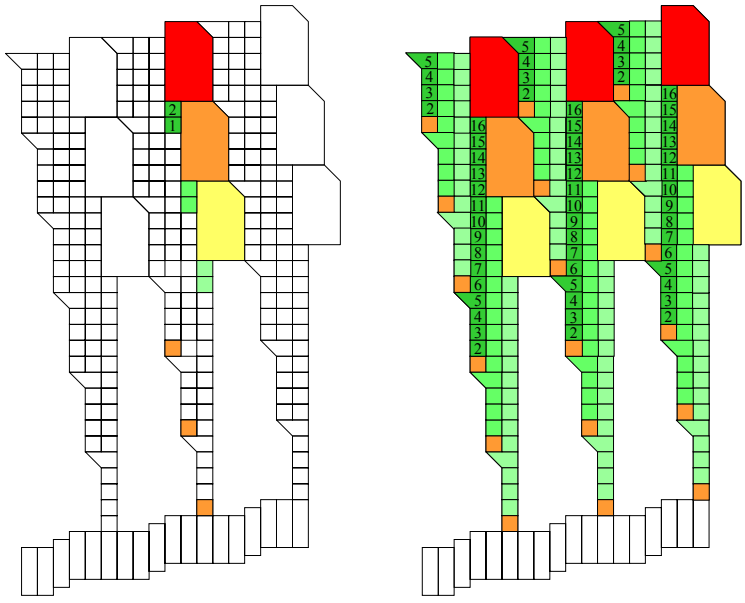
2.2. Operations

2.2.1 Image capturing operation

The image capturing operation is shown in Fig. 3. Fig. 3 (a) and Fig.3 (b) show the states in which the image signals of the first two frames are recorded, and the image signals for the second to the sixteenth frames are recorded, respectively. In the latter case, the image signals for the first frame have already been drained to the outside of the sensor through the drain. The image capturing operation with the overwriting continues until the target event occurs and a trigger signal to stop the image capturing operation is released to the sensor.

2.2.2 Readout operation

After the image capturing operation ceased, the image signals stored in the in-situ storage are readout to a buffer memory outside the sensor and, finally, reconstructed as consecutive image frames. At first, the mage signals stored in the vertical readout CCDs, i.e., the last segments of storage CCD elements, are readout through the horizontal readout CCD. When the vertical readout CCDs become empty, the image signals stored in the storage CCD elements are transferred to the vertical readout CCDs until the vertical readout CCDs are filled with the image signals. The operation is repeated until all the image signals are read out of the sensor and the in-situ storage CCDs become empty.



(a) (b)

Fig. 3 Image capturing operation of the ISIS
(a) Image signals of the first and the second frames are stored in the CCD storage channels.
(b) Image signals of the second to the sixteenth frames are stored in the CCD storage channels. The storage area is full of image signals. The image signals of the first frame have been drained. By the continuous overwriting operation, the latest image signals are always kept within the image sensor until a target event occurs and the trigger signal to cease the continuous recording operation is released to the sensor.

2.3. Example image and requirements for improvements

An example of a captured image is shown in Fig. 4, which is a shockwave reflected by a wall, taken at 1,000,000 fps by Prof. Takayama et al. of the Shockwave Research Institute of Tohoku University. It shows very good image quality.

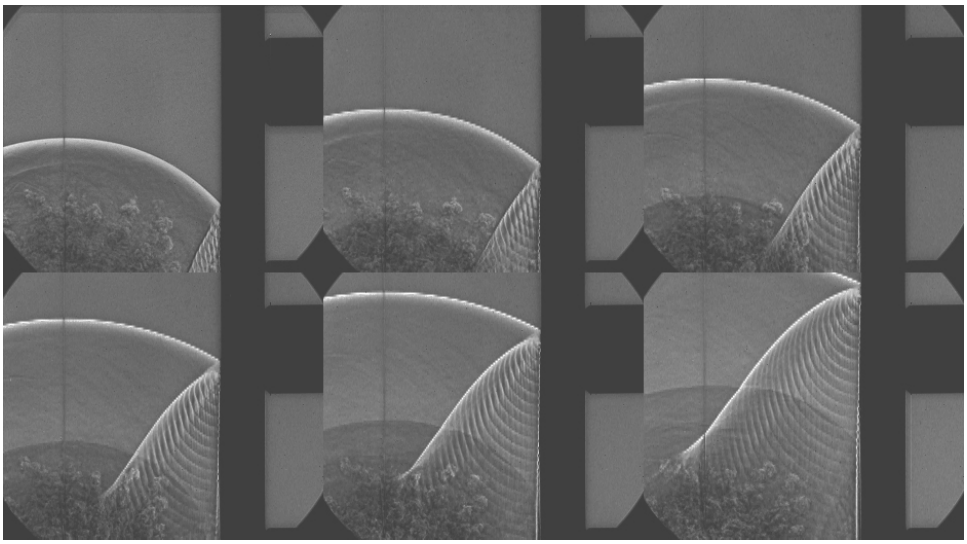


Fig. 4 Shock wave reflected by a wall captured at 1,000,000 fps by Prof. Takayama et al. of Tohoku University

Through various test-applications of the ISIS-V2 camera, improvements are required from the test-users as follows:
(1) Increase of number of consecutive images
(2) Increase of the pixel count
(3) Higher frame rate
(4) Higher sensitivity
(5) Capturing of color images
(6) Development of effective and user-friendly trigger systems
(7) Synchronized image capturing with two or more cameras
(8) Lower price

The improvements to meet some of these requirements are explained in the following sections.

3. AN ULTRA-HIGH-SPEED SENSOR WITH A LARGE FORMAT: ISIS-V3

3.1. Increase of pixel count and the theoretical maximum frame rate

To meet the requirement for increase of the pixel count, the ISIS-V3 was designed, which completed in March 2002. Since, for ultra-high-speed continuous image capturing, many memory elements are installed within or adjacent to each pixel, the pixel size of the ISIS is extraordinarily large. Due to the large pixel size, the pixel count of the ISIS is severely limited. Namely, it is very difficult to realize an image sensor to satisfy both ultra-high-speed and sufficiently large spatial resolution. The simplest way to increase the pixel count is to reduce the pixel size. The other way which was employed in the design of the ISIS-V3 is the three-edge buttable design.

The frame rate of the ISIS was limited by two factors as follows:
(1) Clock frequency of storage CCD
(2) Time required for electrons generated in the photodiode by incident light to reach to the input gate, i.e., the first CCD element of each storage CCD

If electrons generated in the photodiode gather at once at the input gate, the frame interval is equal to the duration for a packet of the electrons, i.e., an image signal, to be transferred from the input gate to the next CCD element. For standard interline-transfer CCD image sensors, very high clock frequency, from 25 MHz to 60 MHz, is applied to the horizontal readout CCD. The transfer scheme is the two-phase transfer, which can transfer charge packets faster, while charge packets per a unit-channel width of the transfer scheme is relatively small. The horizontal readout CCD is installed outside the photo-receptive area, the width can be sufficiently widened. Therefore, the two-phase-transfer is

mainly applied to the horizontal readout CCD. Rather low clock frequency, one to several MHz, with the four-phase transfer scheme is applied to the vertical CCDs in the photo-receptive area to keep charge-handling capacity large. Therefore, if the two-phase transfer is applied to the in-situ storage CCD, the theoretical maximum frame rate of the ISIS is 25-60 Mfps, , and if the four-phase transfer is applied, as used in standard designs, it is one-to-several Mfps.

On the other hand, it takes more than 100 ns for an electron to run from an outer edge of a long photodiode of the ISIS-V2 to the input gate at the other edge. Therefore, the theoretical maximum frame rate estimated from the size and the potential profile of the photodiode of the ISIS=V2 is less than 10 Mfps.

The improvements employed in the design of the ISIS-V3 to increase the pixel count and to increase the theoretical maximum frame rate are explained in this section.

3.2. Pixel structure of the ISIS-V3

A pixel of the ISIS-V3 and examples of the potential profiles in the photodiode area calculated by simulations are shown in Fig. 5 and Fig. 6. One of the major improvements from the ISIS-V2 is that the ISIS-V3 has a square photodiode grid and the CCD grid is slanted, instead. In other words, the ISIS-V3 pixels shown in Fig. 5 were slightly rotated from those of the ISIS-V2 shown in Fig. 1.

The photodiode is covered with two very thin electrodes, i.e., precisely speaking, the photo active area is a photogate. Driving voltages applied to these electrodes can be operated independently from those applied to the electrodes of the storage CCD. This concept was also employed in the design of the ISIS-V2 for higher frame rate. The size of the photodiode is extraordinarily large. The length is 66.3 microns for the ISIS-V2 and 50 microns for the ISIS-V3. It takes a long time for electrons to travel on such a long photodiode.

Very fast electronic shutter was realized by this improvement. When relatively high driving voltages are applied to the electrodes on the photodiodes, electrons generated by incident light are kept in the photodiode; when the voltages become zero, all the electrons are drained to the substrate at once. The driving voltages can be swiftly changed.
The shapes of the electrodes on the photodiode are not rectangular. The second electrode has a shape of a pair of wings, as shown in Fig.5. The width of each wing is decreased toward the edge. The advantage of this improvement can be easily understood by comparison of Fig. 6 (a) and (b). In Fig. 6 (a), different driving voltages, 10 V and 12 V,

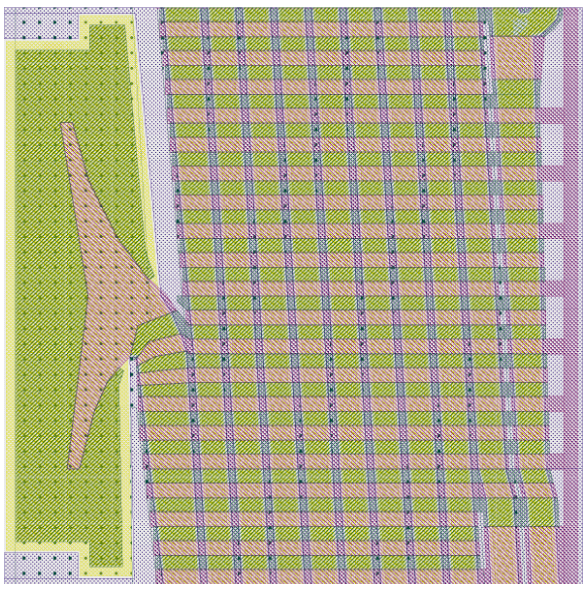


Fig. 5 A pixel of the ISIS-V3 (Two electrodes PG1 and PG2 (Wing-shaped) are placed on the photodiode.

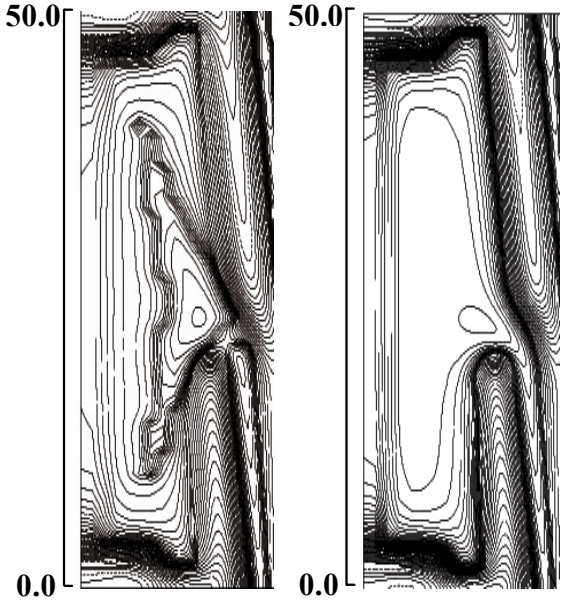


Fig. 6 Potential profiles: (a) left (b) right
(a) PG1: 10V; PG2: 12 V (b) PG1 and PG2: 10V

are applied to the first and the second gates, which generate potential gradient from all the edges to the point where the potential is deepest, locating very close to the input gate. The potential gradient makes electrons generated by incident light smoothly and immediately move to the deepest point. In Fig. 6 (b), the same voltage, 12 V, is applied to both electrodes. In this case, wide area is covered with very flat potential profile. Electrons are trapped by small up-and-down, which is invisible in the simulation results, but actually generated in the fabrication process. Though electrons moves on the up-and-down with free motion by thermal effect toward the input gate, the velocity is seriously decreased.

The potential gradient in the photodiode is generated by the following three reasons:
(1) Strong p-type doping around the photodiode
(2) Difference of the driving voltages applied to the two electrodes
(3) Change of the width of the second electrode

The third effect is explained in Fig. 7. Fig. 7 (a) shows the effect of linearly changing width on the potential gradient. The potential gradient changes, forming exponential curve. Electrons are transferred most efficiently by a linearly changing potential profile, as shown in Fig. 7 (b), since the minimum gradient is maximized by the linear potential profile. The linear potential profile is realized by the width change expressed with the inverse function of the exponential curve, i.e., a logarithmic curve, which is applied to the shape of the wings of the second electrode.

The same concept is also applied to the design of the storage CCD channels, when electron charge packets should be transferred from a deeper point to a shallower point in the potential profile. One example is shown in Fig. 6 (b): the potential in the photodiode near the input gate is deepest; the potential profile of the storage CCD channel starting from the input gate has an adverse linear profile as shown in the right-lower area of the figure.

Many other improvements were introduced. Among them are:
(1) Small pixel size
(2) The input gate was installed at the center of a long photodiode

The width of the storage CCD channels was reduced to 3.0 microns of the ISIS-V3 from 5.1 microns of the ISIS-V2. The length of each storage CCD element was 5.0 microns, which was slightly reduced from that of the ISIS-V2, i.e., 5.1 microns. The reduction rate of the pixel size from the ISIS-V2 was 42.3%. Taking advantage of the smaller pixel size, the pixel count was increased to about 160 kpixels from about 81 kpixels of the ISIS-V2.

As shown in Fig. 5, the first CCD storage element, i.e., the input gate, of the ISIS-V3 was moved to the center of the right edge of the long photodiode form the bottom of the photodiode employed in the ISIS-V2. This improvement

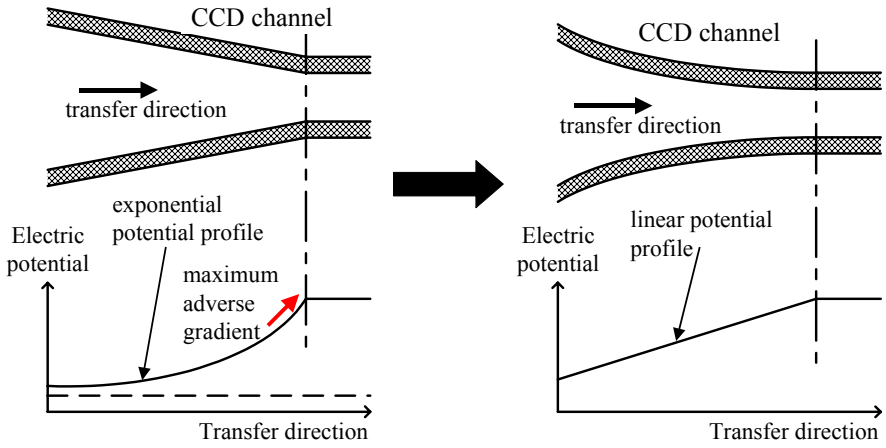


Fig. 7 Effects of change of width on the potential profile
(a) left: Linear change of the width (b) right: Linear potential profile by a logarithmic change of the width

increased the theoretical maximum frame rate. If the pixel size is the same, the distance from the upper or the lower edge of the photodiode to the input gate at the center is a half of that from the upper edge to the bottom, which is the case employed in the design of the ISIS-V2. If the driving voltages applied to the electrodes are the same, potential gradient is doubled by making the distance half, and the traveling velocity of the electrons is doubled. These two effects, i.e., the half distance and the doubled potential gradient, make the traveling time of the electrons one forth, and the theoretical maximum of the frame rate four-time faster. In addition, the length of the photodiode of the ISIS-V3 is shorter than that of the ISIS-V2, the design of the ISIS-V3 achieved a five-time faster frame rate.

Simulation results on the ISIS-V3 showed that the time for an electron generated at the edge of the photodiode to the input gate for the most critical condition, for which the traveling time is maximized, is about 40 nanoseconds. Therefore, precisely speaking, the theoretical maximum frame rate of the ISIS-V3 is 25 Mfps. Practically, by applying post-digital signal processing, the maximum frame rate may reach 100 Mfps.

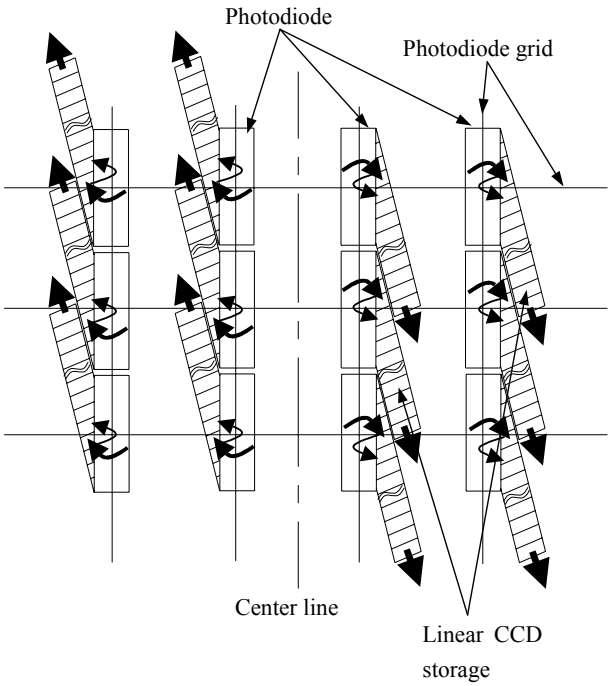


Fig. 8 The ISIS-V3 is buttable along the center line

Subsequently, the improvements on the pixel design of the ISIS-V3, explained above, contribute to both increases of the spatial resolution with the pixel count of about 160 kpixels and the theoretical maximum frame rate of more than 25 Mfps.

3.3. Three-edge buttable design

The square photodiode grid employed in the design of the ISIS-V3 has another advantage. The design is suitable to make buttable chips as shown in Fig. 8. A column of photodiodes has their storage area in one side of the column. Therefore, in one edge area, no storage area exists, which can be the cuttable area. By packaging two chips with one of the chips rotated, we can easily make a sensor with a doubled pixel count. Actually, the ISIS-V3 was designed as three-edge buttable sensor.

This is very much advantageous to realize an image sensor with a large photo-receptive area. The yield rate, i.e., the ratio of the number of the working sensors to that of the fabricated ones seriously decreases, when the chip size is enlarged. For example, if the yield rate of a large chip is 10% or 1%, that of a chip with a doubled area becomes 1% or 0.01%, respectively.

Though the design of the ISIS-V3 completed in March 2002, it has not been fabricated due to the financial problem. However, it became a base of the design of the next-generation ultra-high-speed image sensor, ISIS-V4, as explained in the next section.

4. AN ULTRA-HIGH SPEED IMAGE SENSOR FOR BROADCASTING: ISIS-V4

4.1. Major improvements from ISIS-V3

NHK, the Japan Broadcasting Corporation, is working for development of an ultra-high-speed video camera for broadcasting. For an initial test, they made a color video camera with triple ISIS-V2 sensors, and applied it to broadcasting of sport and scientific programs[3]. The results were very successful. People enjoyed images of balls hit by a baseball bat or a golf club, and commentators' explanations on the relationships of the movements of the balls and the outcomes.

Through the test applications, several requirements for improvements have been collected as follows:
(1) Larger pixel count for HDTV
(2) Higher sensitivity for broadcasting from stadiums under illumination of 2,000 lux
(3) Continuous readout of 2 kfps

It is very difficult to simultaneously satisfy all these requirements. The ISIS-V4 was designed based on the design of the ISIS-V3, to achieve the performance close to the above requirements, by introducing further improvements as follows:
(1) Various smaller improvements to further reduction of the pixel size
(2) Possible introduction of CCM, Charge Carrier Multiplication by Impact Ionization, invented by Hynecek[4)]
(3) Parallel readout with eight readout amplifiers for one chip
(4) Aspect ratio of 16:9 (HDTV format)
(5) Four-sensor camera with Bayer's color filter alignment

The improvement listed in (5) is for the camera design, not for the sensor design. Therefore, it is explained later in the sub-section **4.3.**

The pixel design is basically the same as the ISIS-V3 shown in Fig. 5. The length of the storage CCD elements was reduced to 3.6 microns from 5.0 microns of the ISIS-V3. With the smaller pixel size, the pixel count of one chip was increased to 147, 600 (= 360x410 pixels) pixels from 81,120 pixels of the ISIS-V2, and the number of total consecutive frames was increased to 144 frames from 103 of the ISIS-V2 and 100 of the ISIS-V3. One ISIS-V4 sensor is made of two buttable chips, and makes the pixel count about 300 kpixel (720x410 pixels) and the aspect ratio about 16:9 (720 : 410). The increased number of frames provides reproduction of moving images at 10 fps for 14.4 seconds.

The ISIS-V4 works in parallel-readout mode as well as in the ISIS-mode. Eight readout amplifiers on one chip can realize parallel readout at 1,000 fps to memory device outside the sensor.

In sport broadcasting from sport stadiums, continuous strong illumination for high-speed video imaging is not allowed. To improve the sensitivity of the camera, NHK engineers are working for development of an on-chip micro-lens array. The pixel size of the ISIS is very large, due to large memory area installed to each pixel. Therefore, the micro-lens is very large, which cannot be produced by conventional processes to produce small micro-lenses mounted on standard CCD elements.

Another method which was introduced to the design of the ISIS-V4 for improvement of the sensitivity is the CCM which was invented by Hynecek for efficient amplification of image signals within CCD channels. He utilized impact ionization in the CCD elements for amplification. When very high potential gradient is generated in a CCD channel, impact of over-accelerated electrons on the silicon grid generates the secondary electrons, which can be a noise source. However, repeating very low impact ionization provides linear increase of signals and random noises increasing proportionately to the square of the number of repetition. Therefore, repetition of the weak impact ionization of several hundred times increases the S/N ratio.

In Table 1, major performance indices of the ISIS-V4 is compared with those of the ISIS-V2.

4.2 Package

The design of the ISIS-V4 completed in 2003. The sensor and the camera mounting it are still under development. A photograph of a packaged two chips of the ISIS is shown in Fig. 9.

4.3 Semi-HDTV-format ultra-high-speed video camera

The pixel count of a camera with four ISIS-V4 nominally reaches to about 1.2 Mpixle (2x4x147.6 kpixels). The sensors are attached to the camera in the staggered alignment, composing Bayer's color filter alignment with two green pixels, one red pixel and one blue pixel in a unit of four pixels. Typical broadcasting TV cameras have three sensors which are aligned at the same position and a pixel of each sensor captures green, red and blue lights of the same pixel. An HDTV camera catches images with 2 Mpixel, i.e., the total number of the pixels of the three sensors are 6 Mpixels.

Table 1 Comparison of the ISIS-V2 and the ISIS-V4

	ISIS-V2	ISIS-V4
Frame Rate	1,000,000 fps (max)	1,000,000 fps (max)
Pixel Count	312x260 (=81,120) pixels	(2x360)x410 (=295,200) pixels
Pixel Size	66.3x66.3 microns^2	50.4x50.4 microns^2
Size of CCD Element	5.1x5.1microns^2	3.0x3.6microns^2
Fill Factor (Area of Photogate)	13% (580 microns^2)	16.8% (426.7 microns^2)
Number of Stored Image	103 frames	144 frames
Charge Handling Capacity	25,000 electrons	18,000 electrons
Grey Level	12 bits	12 bits
Overwriting Drain	Installed	
Transfer Scheme	4-phase transfer (Quasi 2-phase transfer for HCCD)	
Temperature of the Sensor	0-5 degree (Cooled by Peltier Device)	
Parallel Readout	none	1,000 fps (2x8 readout taps)
On-chip Micro-lens array	none	Fill factor 50% (under deveropment)
CCM*		installed for test

* Charge Carrier Multiplication by Successive Impact Ionization

About seventy percent of the pixel count of the Bayer's alignment is equivalent to that of the triple-sensor TV camera. Therefore, the ISIS-V4 camera provides the pixel count of about 0.83 Mpixel (0.7x2x360x410 pixels), which is less than a half of the standard HDTV format. Thus, the camera with four ISIS-V4 only provides a semi-HDTV format ultra-high-speed video camera. It is expected that the pixel count will be nearly doubled in the near future by employment of the most advanced CCD technology to further reduce the pixel size.

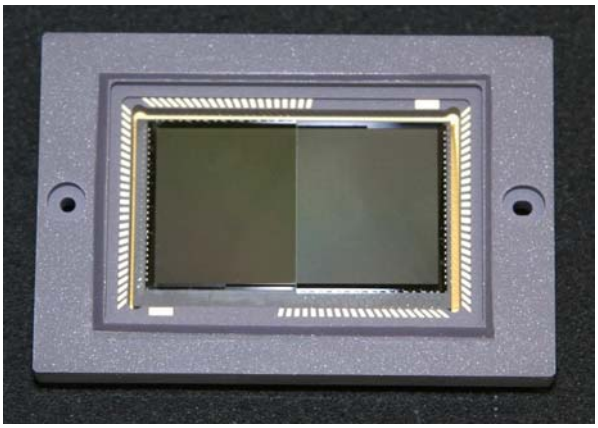


Fig. 9 The packaged ISIS-V4

5. CONCLUDING REMARKS

An ultra-high-speed video camera of 1,000,000 fps with a semi-HDTV format is now under development. The sensor is the ISIS-V4. The history of improvements of the design from the ISIS-V2 to the ISIS-V4 is summarized. Further development is planned to increase the sensitivity of the sensor to a photon-counting level. This is reported elsewhere[5].

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